



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,431	04/27/2006	Renato Confa	69179-230055	5100
26694 7590 04/09/2008				
VENABLE LLP				
P.O. BOX 34385				
WASHINGTON, DC 20043-9998				
EXAMINER				
WITKOWSKI, ALEXANDER C				
ART UNIT		PAPER NUMBER		
4193				
MAIL DATE		DELIVERY MODE		
04/09/2008		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



# Office Action Summary

**Application No.**

10/577,431

**Applicant(s)**

CONTA ET AL.

**Examiner**

ALEXANDER C. WITKOWSKI

**Art Unit**

4193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 April 2006.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-27 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-27 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 04/27/2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO/ISD)  
Paper No(s)/Mail Date 04/27/2006  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_



## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 - 7, 11 - 14, 16 - 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Miki et al. (US 6,554,408).

With respect to claim 1, Miki et al. (US 6,554,408) teaches an **ink jet printhead (col.1, lines 12-13) comprising one or more ejection modules (Fig.1; col.4, line 14), each including a silicon chip (Fig.1: 17), a plurality of ejection nozzles (col.5, lines 61-62) arranged adjacent to an edge of the module (Fig.1: 14, 17), ejection cells (Fig.1: 12) for said nozzles and delivery channels (Fig.1: 13) for the ink of the cells, the above-mentioned head being characterized in that said module or said modules each include a distribution channel (Fig.1: 16) adjacent to the front and in fluid communication with the delivery channels and a nozzle layer (Fig.1: 19), integrated with the relative chip (Fig.1: 17) and in which ejection nozzles are made parallel to the front (Fig.1: 19), said head also comprising:**



**a support for mounting the module or the modules (Fig.1: 18) and which defines a feeding duct (Fig.1: 16) for the ink in fluid communication with said delivery channels (Fig.1: 13); and**

**sealing means between the module or the modules and said support constituting a fluid seal between the feeding duct of the support and the ejection cells of the module or of the modules (col.2, lines 48-54).**

With respect to claim 3, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 1, **characterized in that said distribution channel (Fig.1: 16) is defined by a surface etching in the relative silicon chip (Fig.3E: 35; col.7, lines 18-19).**

With respect to claim 4, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 1, **wherein each chip (Fig.1: 17) defines a reference surface (Fig.1: 18) upon which are arranged the above-mentioned cells, said head being characterized in that the distribution channel of the module or of the modules (Fig.1: 16) is made in an area of a reference surface that includes said front and in which said chip also comprises a series of ribs extending transversally (Fig.1: showing ribs between each ink channel) through the distribution channel and partially bearing the nozzle layer (Fig.1: 19);**

**said sealing means (col.2, lines 48-54) including a sealing lamina having an edge adjacent to the nozzles (Fig.1: 14, 15; Fig.5B: 53, 54, 57) and**



Art Unit: 4193

**mounted to provide fluid sealing between the nozzle layer and said support and to cover the feeding duct** (col.2, lines 48-54) (Fig.3E: 33; Fig.5B: 52, 57).

With respect to claim 5, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 4, **characterized in that said ribs are set adjacent to each delivery channel** (Fig.1: 13: showing ribs between each ink [delivery] channel).

With respect to claim 6, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 4, **characterized in that said ribs are set adjacent to a plurality of delivery channels** (Fig.1: 13: showing ribs adjacent to ink [delivery] channels).

With respect to claim 7, Miki et al. teaches a **head** (col.1, lines 12-13), as applied to claim 4, **characterized in that the nozzle layer** (Fig.1: 19) **defines the ejection cells** (Fig.1: 12) **and the delivery channels** (Fig.1: 13) **and is fastened to the above-mentioned ribs** (Fig.1: 13: showing ribs between each ink [delivery] channel).

With respect to claim 11, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 1, **wherein the cells** (Fig.1: 12) **and the delivery channels** (Fig.1: 13) **rest upon a given surface of said chip** (Fig.1: 17), **said head being characterized in that, in said module or in each module, the**



Art Unit: 4193

**distribution channel (Fig.1: 16) is made on a surface of the chip opposite said given surface, facing the feeding duct (Fig.1: 16; ink inlet 16 is identical to applicants' feeding duct) of the mounting support and wherein ducts or slots are provided, passing through said chip which provide fluid connection between the distribution channel on said opposite face and the delivery channels on said given surface (Fig.1: 13, 16, 17).**

With respect to claim 12, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 11, **characterized in that said nozzle layer (Fig.1: 19) acts as a fluid seal for said cells (Fig.1: 12) and for said channels (Fig.1: 13, 16) with respect to said given surface of the chip** (col.2: lines 48-52).

With respect to claim 13, Miki et al. teaches a **printhead** (col.1, lines 12-13) **according to claim 11, characterized in that said distribution channel (Fig.1: 16) is adjacent to said front (Fig.1), has no bank and defines in the chip (Fig.1: 17) a projecting section of lesser thickness and in which said nozzle layer (Fig.1: 19) extends over said projecting section** (col.4, lines 29-37).

With respect to claim 14, Miki et al. teaches a **printhead** (col.1, lines 12-13) **according to claim 11, characterized in that said sealing means include sealing material inserted between the nozzle layer (Fig.1: 19) and / or the**



**chip (Fig.1: 17) and said support (Fig.1: 18) (col.2: lines 48-52).**

With respect to claim 15, Miki et al. teaches all the limitations of claim 1. However, Miki et al., does not teach **that said nozzle layer defines spaces above the substrate for a height of 10 - 25 micrometer in said cells and in said delivery channels.** It would have been an obvious design choice to one of ordinary skill in the art at the time that this invention was made for the nozzle layer to define spaces above the substrate for a height of 10 - 25 micrometer in cells and in delivery channels in order to more effectively utilize the surface and thickness of the chip.

With respect to claim 16, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 1, **characterized in that it may be used in a parallel or serial-parallel type printing device and comprises a plurality of modules (Fig.1; col.4, line 14) aligned along said front (Fig.1) and in which said support (Fig.1: 18) comprises a board of rigid material that defines said feeding duct (Fig.1: 16) through its thickness; and in which said modules are mounted side by side on said board (col.4, lines 28-37: describing Fig.1 as illustrating a plurality of ejection modules) and with the nozzles (Fig.1: 14, 15) aligned parallel (Fig.1) to the front.**

With respect to claim 17, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim 16, **characterized in that it includes a frame (Fig.1: 18)**



**mounted on said board beside said ejector modules (Fig.1; col.4, line 14), having the upper surface adjacent to the upper surface of the nozzle layers (Fig.1: 19) of the above-mentioned modules.**

With respect to claim 18, Miki et al. teaches a **printhead** (col.1, lines 12-13) **according to claim 4, characterized in that the upper surface of the frame (Fig.1: 18) is substantially flush with the upper surface of the nozzle layers (Fig.1: 19) and wherein said sealing lamina is mounted tight on the frame and on the nozzle layers of the modules (col.2: lines 48-52), in correspondence with the above-mentioned ribs (Fig.1: 13: showing ribs between each ink channel).**

With respect to claim 19, Miki et al. teaches a **printhead** (col.1, lines 12-13) **according to claim 11, characterized in that said sealing material is arranged between said frame (Fig.1: 18) and the nozzle layer (Fig.1: 19) or the relative chip of the modules (Fig.1: 17) (col.2: lines 48-52).**

With respect to claim 20, Miki et al. teaches a **process for manufacturing an ink jet printhead** (col.1, lines 12-13), **comprising the step of preparing ejector modules (Fig.1; col.4, line 14), each including a chip substrate (Fig.1: 17) with a relative front having a plurality of resistors, ejection cells (col.5, lines 61-62) and delivery channels (Fig.1: 13) for the ink of the cells, said process being characterized in that the modules each**



**include a distribution channel (Fig.1: 16) in fluid connection with the delivery channels and a nozzle layer (Fig.1: 19) having ejection nozzles (col.5, lines 61-62) aligned with said front and arranged above the resistors and in which the head includes a support (Fig.1: 18) having an ink feeding duct (Fig.1: 16) for one or more modules; the assembling of the head including the steps of:**

**mounting the module or modules on said support so as to have the distribution channel (Fig.1: 16) or channels in fluid communication with said feeding duct (col.2, lines 48-54);**

**and hydraulically sealing the nozzle layer of the module or of the modules from said support, for ink-tightness in feeding the ink between the feeding duct and the nozzles through said delivery channels (col.2, lines 48-52).**

With respect to claim 21, Miki et al. teaches a **process**, as applied to claim 20, **characterized in that the manufacturing process of the modules includes steps of:**

**making an etching on a given face of the chip to produce said distribution channel (Fig.1: 16) between the front and an area adjacent to the resistors (Fig.1: 21) and parallel to the front; producing sacrificial volumes (Figs.3A-3E) defining the limits of the ejection cells (Fig.1: 12) above the said resistors (Fig.1: 21) and the delivery channels (Fig.1: 13) above the said area;**



**applying a structural layer over said sacrificial volumes to define said nozzle layer (Fig.1: 19);**

**and producing the ejection nozzles (col.5, lines 61-62) on said structural layer in correspondence with the sacrificial volumes of the cells.**

With respect to claim 22, Miki et al. teaches a **process**, as applied to claim 21, **characterized in that said etching produces on said face, in addition to the distribution channel (Fig.1: 16), a series of ribs which extend transversally (Fig.1: showing ribs between each ink channel) in said channel and in which a part of the sacrificial volumes (Figs.3A-3E) extends into the space between said ribs and on said channel and a part of the structural layer is applied on the ribs and remains fastened on said ribs after removal of the sacrificial volumes.**

With respect to claim 23, Miki et al. teaches a **process**, as applied to claim 22, **characterized in that said step of producing sacrificial volumes (Figs.3A-3E) includes the sub-steps of:**

- (a) covering said distribution channel (Fig.1: 16) with sacrificial photoresist, flush with said data face of the chip;**
- (b) planarizing the photoresist covering the channel and cleaning the parts adjacent to said distribution channel;**



**(c) applying a layer of controlled thickness of sacrificial photoresist on said substrate above the resistors (Fig.1: 21), the ribs (Fig.1: showing ribs between each ink channel) and the photoresist covering the channel;**

**(d) exposing with a mask said layer of controlled thickness for defining said cells, the delivery channels (Fig.1: 13) and the distribution channel and delimiting said ribs; and**

**(e) developing said layer of controlled thickness constituting the sacrificial volumes for said cells, for the delivery channels and for the distribution channel and leaving zones for attachment of the chip beside said cells and the distribution channels and on said ribs.**

With respect to claim 24, Miki et al. teaches a **process**, as applied to claim 20, characterized in that said longitudinal etching is made on the face of the chip, opposite the said given face, forming a projecting section delimited by the said front and in which a slot forming step is provided, in which slots are produced in the thickness of the projecting sections and in correspondence with the delivery channels (Fig.1: 13) and in which, for assembling of the head, the modules are mounted on the bearing surface of the support (Fig.1: 18) with said slots in fluid connection with the feeding duct of the support.

With respect to claim 25, Miki et al. teaches a **process for manufacturing a head**, as applied to claim 20, characterized in that said



Art Unit: 4193

**support (Fig.1: 18) includes a board with a bearing surface for said chips (Fig.1: 17) and an upper surface adjacent to the feeding duct and a distance from said bearing surface and wherein said upper surface is defined by a frame or is obtained directly from the board, the sealing step including the insertion of sealing means between the chip or the structural layer and said upper surface (col.2, lines 48-54).**

With respect to claim 26, Miki et al. teaches a **process**, as applied to claim 22, **characterized in that said sealing means include a sealing lamina glued between said upper surface and the structural layer, in contrast with said ribs (col.2, lines 48-54).**

With respect to claim 27, Miki et al. teaches a **process**, as applied to claim 24, **characterized in that said sealing means include sealing material inserted between the fronts of the chips (Fig.1: 17) and said upper surface (col.2, lines 48-54).**

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.



Claims 2, 9, 10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. (US 6,554,408).

With respect to claim 2, Miki et al. teaches all the limitations of claim 1. However, Miki et al. does not teach **that, in said module or in each module the ejection cells are positioned at 0.5 - 1.0 mm from said front.** It would have been an obvious to one of ordinary skill in the art at the time that this invention was made for the ejection cells in the module or in each module to have been positioned at 0.5 - 1.0 mm from the front, because it would have been an obvious choice of design and recognizable by one of ordinary skill in the art in order to more effectively utilize the surface and thickness of the chip.

With respect to claim 9, Miki et al. teaches all the limitations of claim 4. However, Miki et al. does not teach **that the distribution channel is of width 0.3 - 1.0 mm and said ribs extend for a distance of 0.2 - 1.0 mm in said distribution channel.** However, it would have been an obvious design choice to one of ordinary skill in the art at the time that this invention was made to make the distribution channel of width 0.3 - 1.0 mm and the ribs to extend for a distance of 0.2 - 1.0 mm in the distribution channel because it would have been an obvious choice of design and recognizable by one of ordinary skill in the art in order to more effectively utilize the surface and thickness of the chip.



With respect to claim 10, Miki et al. teaches all the limitations of claim 4. However, Miki et al. does not teach **that said ribs are of width 15-30 micrometer**. However, it would have been to one of ordinary skill in the art at the time that this invention was made to make the ribs of width 15-30 micrometers because it would have been an obvious choice of design and recognizable by one of ordinary skill in the art in order to more effectively utilize the surface and thickness of the chip.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. (US 6,554,408) in view of Bartky et al. (US 4,879,568).

5. With respect to claim 8, Miki et al. teaches all the limitations of the base claims 4 - 7. However, Miki et al. does not teach that **the sealing lamina is limited by a tapering edge adjacent to said nozzles**.

Bartley et al. teaches the sealing lamina is limited by a tapering edge adjacent to said nozzles (col.9, lines 60-63).

It would have been obvious to one of ordinary skill in the art at the time of this invention to modify Miki et al. to provide a sealing lamina on one side of a channel that is limited by a tapering edge adjacent to the nozzles, as taught by Bartky et al., for the purpose of improving bonding on the tapered side of the channel.



***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Miyata et al. (US 6,616,270) discusses an ink jet print head and an channel forming substrate to effect delivery of ink to nozzles.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEXANDER C. WITKOWSKI whose telephone number is (571)270-3795. The examiner can normally be reached on Monday - Friday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Long Nguyen can be reached on 571-272-1753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Art Unit: 4193

ACW

/Taghi T. Arani/

Supervisory Patent Examiner, Art Unit 4193

/4/5/2008